SYMMETRICAL HIGH FREQUENCY SCR STRUCTURE AND METHOD

Abstract of the Disclosure

In one embodiment, an SCR device (41) includes a p+ wafer (417), a p- layer (416), an n+ buried layer (413), and an n- layer (414). P- wells (411,421) are formed in the n- layer (414). N+ regions (412,422) and p+ regions (415,425) are formed in the p- wells (411,421). A first ohmic contact (431) couples one n+ regions (422) to one p+ region (425). A second ohmic contact (433) couples another n+ region (412) to another p+ region (415) to provide physically and electrically symmetrical low-voltage p-n-p-n silicon controlled rectifiers. A deep isolation trench (419) surrounding the SCR device (41) and dopant concentration profiles provide a low capacitance SCR design for protecting high frequency integrated circuits from electrostatic discharges.